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EXAMINER	
NGUYEN, NHA T	
ART UNIT	**PAPER NUMBER**
2825	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/558,842	CHENG ET AL.	
	Examiner	Art Unit	
	NHA T. NGUYEN	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/21/2006, 9/25/2006, 9/24/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Application filed on 11/29/2005 and IDS filed on 4/21/2006, 9/25/2006, and 9/24/2008.

Claims 1-26 are pending.

Drawings

2. Figures 1, 2, 3A, 3B are objected to are objected to as failing to comply with 37 CFR 1.84(I) because every line, number, and letter must be durable, clean, black (except for color drawings), sufficiently dense and dark, and uniformly thick and well-defined in the drawings.

In Figures 4, it not clear what Y axis represent – Y axis is not labeled. In Figures 5A and 5B, X and Y axis are not labeled.

Specification

3. The disclosure is objected to because of the following informalities:

Para [0017] of the disclosure include reference by using a hyperlink. An incorporation by reference by hyperlink or other form of browser executable code is not permitted. See MPEP 608.01(p)

Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-24 are non-statutory because a § 101 process claim must (1) be tied to another statutory class (a particular machine or apparatus) or (2) transform underlying subject matter (such as an article or materials) to a different state or thing; see In Re Bilski, 545 F.3d 943, 88 USPQ2d 1385 (Fed. Cir. 2008). If neither of these requirements are met by the claim, the method is not a patent eligible process under § 101.

A § 101 process claim that would not qualify as a statutory process would be a claim that recites purely mental step(s) that can be performed manually or merely manipulating an abstract idea without the use of a specific structure. Thus, to qualify as a § 101 statutory process, the claimed step(s) must explicitly recite the other statutory class such as machine (i.e., the computer, the thing) to which it is tied, for example by identifying the machine/computer that accomplishes the step(s) and providing transformation underlying subject matter to a different state or thing to provide meaningful, reasonable limits and a practical application.

Claims 1, 14, and 22 recites a series of process steps for analyzing a circuit network but the steps neither explicitly recite a specific machine/computer that implements the claimed steps nor identify transformation of underlying subject matter to a different state or thing. The claims recited steps of grid construction, and representation of nodes in a matrix, and smoothing operation that can be done on paper

by solving a matrix. As such, the subject matter of claim 1-24 is non-statutory and not patent eligible.

Claims 2-13, 15-21, 23, and 24 are rejected because they depend directly or indirectly from claim 1, 14, and 22.

In order to comply with the 35 USC § 101 statutory requirement, a limitation, i.e., “by using a computer” must be inserted in one of the claimed steps of claims 1, 14, and 22. This would overcome the 35 USC § 101 non-statutory rejection. This would overcome the 35 USC § 101 non-statutory rejection as long as the disclosure support "a computer”

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 14 recited representing a circuit using network by using a matrix of nodes. It is not apparent what the nodes of the matrix represent in relation to the circuit.

Claims 22 and 25 recited representative of a circuit network to construct a plurality of matrices. It is not apparent what the matrices represent, it is not apparent what the parameter or nodes of the matrices represent.

Claims 1, 14, 22, and 25 recited analyzing a circuit, that includes represent a circuit using matrix, perform restriction mapping, interpolation mapping, and smoothing - but it is not clear what is analyze in the circuit. It is not clear what is obtained from the restriction, interpolation, and smoothing of the matrices.

As per claims 2-13, 15-21, 23, and 24 are rejected to for incorporating the above limitations into the claims by dependency.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-9, 12-14, 16, 17, 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kozhaya et al. ("Multigrid-like Technique for Power Analysis", by Joseph N. Kozhaya, Sani R. Nassif, and Farid N. Najm, pages 480-487, @2001 IEEE).

As per claim 1, Kozhaya discloses:

A method for analyzing a circuit network, comprising:

representing a circuit network by using a matrix of nodes having fine nodes and coarse nodes (See Kozhaya, Page 480, i.e. algebraic multigrid, See Pages 482-485, i.e. section 3 – Multi-grid analysis);

applying an adaptive coarse grid construction procedure to assign grid nodes in the matrix as either coarse grid nodes or fine grid nodes according to (1) circuit activities and (2) a matrix structure of the matrix to construct a plurality of levels of grids with different numbers of nodes to respectively represent the circuit network (See Page 480, Section 2, i.e. fine and coarse, Pages 482-485, i.e. section 3 – Multi-grid analysis); and

applying iterative smoothing operations at selected local fine grids corresponding to active regions at a finest level obtained in the adaptive coarse grid construction procedure (See Page 480-481, Section 2, i.e. smoothing…relaxation running few iteration, Pages 482-485, i.e. section 3, i.e. smooth the error).

As per claim 2, Kozhaya discloses all of the steps of claim 1 as discloses above wherein Kozhaya also discloses wherein the coarse grid nodes are divided into non-adaptive coarse nodes which are selected according to the matrix structure, and adaptive coarse nodes which are selected according to circuit activities (See Page 480, Section 2, i.e. fine and coarse, Pages 482-485, i.e. section 3 – Multi-grid analysis).

As per claim 3, Kozhaya discloses all of the steps of claim 2 as discloses above wherein Kozhaya also discloses wherein, in assigning non-adaptive coarse nodes, a node with a maximum potential in its degree is selected as a first non-adaptive coarse node and each neighboring node of the first non-adaptive coarse node is temporality assigned as a fine node, and wherein a potential of each neighboring node of the first non-adaptive coarse node is increased by one unit before a next level of assigning

coarse and fine grid nodes so that each fine node has at least one neighboring coarse node upon completion of assigning non-adaptive coarse nodes (See Page 480, Section 2, i.e. fine and coarse, Pages 482-485, i.e. section 3 – Multi-grid analysis, Page 482, i.e. neighbors of node).

As per claim 4, Kozhaya discloses all of the steps of claim 2 as discloses above wherein Kozhaya also discloses wherein an adaptive coarse node is selected according to a first-order derivative of a nodal voltage (See Page 480, Introduction, i.e. node of voltages, Pages 481-485, i.e. section 2 & 3, i.e. interpolation…voltage node).

As per claim 5, Kozhaya discloses all of the steps of claim 4 as discloses above wherein Kozhaya also discloses wherein a coarse node is selected as an adaptive coarse node when the first-order derivative the coarse node is greater than a threshold value (See Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis).

As per claim 6, Kozhaya discloses all of the steps of claim 5 as discloses above wherein Kozhaya also discloses selecting adaptive coarse nodes in a level that is not the finest level (See Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis).

As per claim 7, Kozhaya discloses all of the steps of claim 1 as discloses above wherein Kozhaya also discloses after the iterative smoothing operations in a level, further comprising: applying a restriction mapping of nodes in the level to a next level

with less nodes; performing iterative smoothing operations again at the next level; and repeating the restriction mapping and the iterative smoothing operations until reaching a level of nodes which are solvable by a direct matrix solving method such as a Gaussian elimination method (See Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis…restriction operator).

As per claim 8, Kozhaya discloses all of the steps of claim 1 as discloses above wherein Kozhaya also discloses after the iterative smoothing operations in a level, further comprising: applying an interpolation mapping of nodes in the level to a next level with more nodes; performing iterative smoothing operations again at the next level; and repeating the interpolation mapping and the iterative smoothing operations until reaching the finest level of nodes (See Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis…interpolation operator).

As per claim 9, Kozhaya discloses all of the steps of claim 8 as discloses above wherein Kozhaya also discloses computing a residual value of an error after the iterative smoothing operations at the finest level; comparing the residual value to a pre-determined threshold; terminating any further processing when the residual value is less than the threshold; and when residual value is greater than the threshold, the method further comprising (See Kozhaya, Pages 481, i.e. residual compare to the error, Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis…restriction operator):

applying a restriction mapping of nodes in the finest level to a next coarser level with less nodes, performing iterative smoothing operations again at the next coarser level; and repeating the restriction mapping and the iterative smoothing operations until reaching a coarsest level of nodes which is solvable by a direct matrix solving method such as a Gaussian elimination method, applying an interpolation mapping of nodes in the coarsest level to a next finer level with more nodes, performing iterative smoothing operations at the next finer level, repeating the interpolation mapping and the iterative smoothing operations until reaching the finest level of nodes, and repeating the restriction mapping, the interpolation mapping and the respective iterative smoothing operation at different levels until the residual value at the finest level is less than the threshold (See Kozhaya, Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis…restriction operator…interpolation operator).

As per claim 12, Kozhaya discloses all of the steps of claim 1 as discloses above wherein Kozhaya also discloses in a passive linear circuit, applying different models to passive circuits exhibiting resistance and capacitance without inductance and passive circuits exhibiting inductance (See Kozhaya, Page 480-481, i.e. linear RC network, See Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis).

As per claim 13, Kozhaya discloses all of the steps of claim 12 as discloses above wherein Kozhaya also discloses separating nodal voltages and branch currents into different vectors during processing to make a system matrix to be symmetric and

positive definite (See Kozhaya, Page 480-481, Introduction, i.e. vector nod voltage…source current, See Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis).

As per claim 14, Kozhaya discloses:

A method for analyzing a circuit network, comprising:

representing a circuit network by using a plurality of levels of grids with different numbers of nodes to represent the circuit network according to an algebraic multigrid method (See Kozhaya, Page 480, i.e. algebraic multigrid, See Pages 482-485, i.e. section 3 – Multi-grid analysis);

applying a restriction mapping from one level to a next coarser level to propagate computation results of the one level to the next coarse level (See Kozhaya, Pages 481-483, Section 2 & section, i.e. restriction operator);

applying an interpolation mapping from one level to a next finer level to propagate computation results of the one level to the next finer level (See Kozhaya, Pages 481-485, Section 2 & Section, i.e. interpolation operator, Section 3.2 – interpolation);

performing an iterative smoothing operation at each level to obtain computation results of each level comprising states of nodes in each level (See Page 480-481, Section 2, i.e. smoothing…relaxation running few iteration, Pages 482-485, i.e. section 3, i.e. smooth the error); and

repeating (1) the restriction mapping and the iterative smoothing operation from the finest level to the coarsest level and (2) the interpolation mapping and the iterative

smoothing operation from coarsest level back to the finest level for at least one time to obtain a solution to the circuit network (See Page 482, i.e. repeatedly coarsening, See Pages 481-485, Section 2 & Section 3, i.e. iterative method…smoothing).

As per claim 16, Kozhaya discloses all of the steps of claim 14 as discloses above wherein Kozhaya also discloses wherein at least one level includes nodes corresponding to only selected circuit regions in the circuit network that are active and does not include nodes corresponding to inactive circuit regions in the circuit network (See Kozhaya, Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis, See Page 482, Grid reduction , i.e. default node…corner nodes).

As per claim 17, Kozhaya discloses all of the steps of claim 14 as discloses above wherein Kozhaya also discloses assigning regions in the finest level with nodes corresponding to active circuit regions in the circuit network as active local fine grids; and performing the iterative smoothing operation only in the active local fine grids in the finest level to obtain computation results of the finest level (See Kozhaya, Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis, See Page 482, Grid reduction , i.e. default node…corner nodes).

As per claim 19, Kozhaya discloses all of the steps of claim 14 as discloses above wherein Kozhaya also discloses applying an adaptive coarse grid construction procedure to assign grid nodes in the matrix as either coarse grid nodes or fine grid

nodes (See Page 480, Section 2, i.e. fine and coarse, Pages 482-485, i.e. section 3 – Multi-grid analysis).

As per claim 20, Kozhaya discloses all of the steps of claim 19 as discloses above wherein Kozhaya also discloses wherein a coarse node is assigned by: assigning a node with a maximum potential to its degree as a first coarse node and all neighboring nodes as initial fine nodes; for each of the initial fine nodes, increasing a potential of each of neighboring nodes by one unit; assigning a node which has a maximum potential among other nodes except for the first coarse node as a second coarse node; and repeating the assigning for nodes that are not assigned as coarse nodes until all nodes are assigned (See Page 480, Section 2, i.e. fine and coarse, Pages 481-485, i.e. section 3 – Multi-grid analysis, Page 482, i.e. neighbors of node).

As per claim 21, Kozhaya discloses all of the steps of claim 19 as discloses above wherein Kozhaya also discloses wherein the coarse nodes are selected according to their values of a first-order derivative of a nodal voltage (See Page 480, Introduction, i.e. node of voltages, Pages 481-485, i.e. section 2 & 3, i.e. interpolation…voltage node).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10, 11, 15, 18, 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozhaya et al. ("Multigrid-like Technique for Power Analysis", by Joseph N. Kozhaya, Sani R. Nassif, and Farid N. Najm, pages 480-487, @2001 IEEE) in view of Brandt ("Multi-level adaptive solutions to Boundary-Value problems", by Achi Brandt, Mathematics Of Computation, Vol 31, Number 138, Pages 333-390, April 1977).

As per claim 10, Kozhaya discloses all of the steps of claim 1 as discloses above. Kozhaya does not discloses the features: dynamically changing designations of active and inactive regions of the circuit network according to circuit activities at different times.

However, Brandt discloses the above features (See Brandt, Page 334, i.e. increasing fineness, See Page 357, i.e. adaptivity of grid, See Page 363-370, i.e. adaptive discretization).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to use the above feature because it allow local smoothness of the solution, and reduce the size of the algebraic system.

As per claim 11, Kozhaya and Brandt discloses all of the steps of claim 10 as discloses above wherein Brandt also discloses applying iterative smoothing operations

in active regions more frequently in time than in inactive regions (See Brandt, Page 334, i.e. increasing fineness, See Page 357, i.e. adaptively of grid, See Page 363-370, i.e. adaptive discretization).

As per claim 15, Kozhaya discloses all of the steps of claim 1 as discloses above. Kozhaya does not discloses the features: wherein the coarsest level is a level where a matrix equation for nodes in the level is solvable by a direct matrix method such as the Gaussian elimination method.

However, Brandt discloses the above features (See Brandt, Page 338-389, i.e. Gauss relaxation).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to use the above feature because it allow local smoothness of the solution, and reduce the size of the algebraic system.

As per claim 18, Kozhaya discloses all of the steps of claim 14 as discloses above, wherein Kozhaya also discloses assigning regions in a level with nodes corresponding to active circuit regions in the circuit network as active local grids and other regions in that level as in inactive grids (See Kozhaya, Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis, See Page 482, Grid reduction , i.e. default node…corner nodes).

Kozhaya does not discloses the features: performing the interactive smoothing operation in an active local grid more frequently than in an inactive grid.

However, Brandt discloses the above features (See Brandt, Page 334, i.e. increasing fineness, See Page 357, i.e. adaptivity of grid, See Page 363-370, i.e. adaptive discretization).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to use the above feature because it allow local smoothness of the solution, and reduce the size of the algebraic system.

As per claim 22, Kozhaya discloses:

A method for analyzing a circuit network, comprising:

applying an algebraic multigrid method to a matrix representative of a circuit network to construct a plurality of matrices with different degrees of coarsening grids (See Kozhaya, Page 480, i.e. algebraic multigrid, See Pages 482-485, i.e. section 3 – Multi-grid analysis);

representing regions in the circuit network exhibiting active circuit activities with active grids and regions in the circuit network exhibiting less active circuit activities with inactive grids (See Page 480, Section 2, i.e. fine and coarse, Pages 482-485, i.e. section 3 – Multi-grid analysis); and

performing an iterative smoothing operation (See Page 480-481, Section 2, i.e. smoothing…relaxation running few iteration, Pages 482-485, i.e. section 3, i.e. smooth the error).

Kozhaya does not explicitly discloses the features: smoothing operation in an active grid more frequently than in an inactive grid to reduce an amount of computation.

However, Brandt discloses the above features (See Brandt, Page 334, i.e. increasing fineness, See Page 357, i.e. adaptivity of grid, See Page 363-370, i.e. adaptive discretization).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to use the above feature because it allow local smoothness of the solution, and reduce the size of the algebraic system.

As per claim 23, Kozhaya and Brandt discloses all of the steps of claim 22 as discloses above wherein Kozhaya also discloses applying a restriction mapping of nodes in a coarse grid to a next coarser grid (See Kozhaya, Pages 481-483, Section 2 & section, i.e. restriction operator); performing the iterative smoothing operation at the next coarser grid (See Page 480-481, Section 2, i.e. smoothing…relaxation running few iteration, Pages 482-485, i.e. section 3, i.e. smooth the error); and repeating the restriction mapping and the iterative smoothing operation until reaching the coarsest grid which has a matrix equation that is solvable by a direct matrix solving method (See Page 482, i.e. repeatedly coarsening, See Pages 481-485, Section 2 & Section 3, i.e. iterative method…smoothing). Wherein Brandt discloses direct matrix solving method such as a Gaussian elimination method (See Brandt, Page 338-389, i.e. Gauss relaxation).

As per claim 24, Kozhaya and Brandt discloses all of the steps of claim 22 as discloses above wherein Kozhaya also discloses applying an interpolation mapping of nodes in one grid to a next finer grid; performing the iterative smoothing operation at the

next finer level; and repeating the interpolation mapping and the iterative smoothing operation until reaching the finest grid (See Kozhaya, Pages 481-485, Section 2 & Section, i.e. interpolation operator, Section 3.2 – interpolation).

As per claim 25, Kozhaya discloses:

An article comprising a machine-readable medium (See Kozhaya, Section 4, Page 485-486) that stores machine-executable instructions, the instructions causing a machine to:

apply an algebraic multigrid method to a matrix representative of a circuit network to construct a plurality of matrices with different degrees of coarsening grids (See Kozhaya, Page 480, i.e. algebraic multigrid, See Pages 482-485, i.e. section 3 – Multi-grid analysis);

divide the circuit network into active regions and inactive regions according to circuit activities (See Page 480, Section 2, i.e. fine and coarse, Pages 482-485, i.e. section 3 – Multi-grid analysis); and

perform an iterative smoothing operation (See Page 480-481, Section 2, i.e. smoothing…relaxation running few iteration, Pages 482-485, i.e. section 3, i.e. smooth the error)

Kozhaya does not explicitly discloses the features: smoothing operation in an active grid more frequently than in an inactive grid to reduce an amount of computation.

However, Brandt discloses the above features (See Brandt, Page 334, i.e. increasing fineness, See Page 357, i.e. adaptivity of grid, See Page 363-370, i.e. adaptive discretization).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to use the above feature because it allow local smoothness of the solution, and reduce the size of the algebraic system.

As per claim 26, Kozhaya and Brandt discloses all of the steps of claim 25 as discloses above wherein Kozhaya also discloses wherein the machine-executable instructions further comprise instructions that cause the machine to perform an iterative smoothing operation to solve for a matrix equation of each grid and to map a computation result of each grid to a next finer or coarser grid (See Page 480-481, Section 2, i.e. smoothing…relaxation running few iteration, Pages 482-485, i.e. section 3, i.e. smooth the error) until a residual error of a solution is less than a pre-determined threshold (See Kozhaya, Pages 481, i.e. residual compare to the error, Pages 481-485, i.e. section 2 & 3, i.e. multi-grid analysis…restriction operator).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to NHA T. NGUYEN whose telephone number is (571)270-

1405. The examiner can normally be reached on M-F 8:30 - 6:00 PM EST. (Every other Friday OFF).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/
Primary Examiner, Art Unit 2825

/N. T. N./
Examiner, Art Unit 2825